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14. ABSTRACT
The original goals for the research program were to: 1) fabricate an interconnected array of single wall carbon nanotubes (SWNT) and 2) use the device to investigate cellular signaling in live cells. The most challenging part of this research (as anticipated) was the fabrication of the carbon nanotube array and most of the effort of this seed program was focused on this part. The interconnect fabrication was completed. A sample device without carbon nanotubes was packaged and tested with living cells to test the interface with optical microscopes and signal electronics. The most difficult part of fabricating an interconnected array of SWNTs is accurately growing or assembling them (with known properties) on interconnects. It was discovered that this could be achieved with a self-assembly technique that is compatible with traditional lithography and processing that is used in manufacturing. This groundbreaking discovery will yield many applications for biological devices and integrated circuits using nanotubes.

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NANOSCALE APPLICATION FOR CARBON NANOTUBE ARRAYS

AFOSR GRANT: FA9550-05-1-0461
FINAL REPORT

AUGUST 31, 2007

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I. SUMMERY

The original goals for the research program were to: 1) fabricate an interconnected array of single wall carbon nanotubes (SWNT) and 2) use the device to investigate cellular signaling in live cells. The most challenging part of this research (as anticipated) was the fabrication of the carbon nanotube array and most of the effort of this seed program was focused on this part. The interconnect fabrication was completed. A sample device without carbon nanotubes was packaged and tested with living cells to test the interface with optical microscopes and signal electronics. The most difficult part of fabricating an interconnected array of SWNTs is accurately growing or assembling them (with known properties) on interconnects. It was discovered that the nanotubes can be assembled on the interconnects using lithography that is much less demanding than previously reported or anticipated in the original proposal. This groundbreaking discovery will yield many applications for biological devices and integrated circuits using nanotubes. The main advantage is that the requirements on the lithography may be relaxed to the point where traditional manufacturing technology may be used to fabricate the device. This is a disruptive technology in that it may significantly shorten the timeline for the introduction of many nanotube devices that would otherwise have to wait for the introduction of lithography that is at the end of the current roadmap for semiconductor technology. The result of this research program may be to reduce the development costs for nanotube devices by hundreds of millions of dollars.

II. ACCOMPLISHMENTS

Wafer Processing and Assembly

Chemical vapor deposition (CVD) has become the method of choice for growing vertically aligned SWNTs.[1] The requirements of SWNT growth in this research are very different from those widely reported in the literature. Mainly because the absolute number of SWNTs needed on a wafer will be several orders magnitude less than most applications. Also, the height of the individual SWNTs will be less than 1 μm. So, rapid high-density growth of very long SWNTs is not a requirement for the proposed device. The most important requirements are for individual vertically aligned SWNTs with uniform and reproducible physical properties. Quartz was chosen as a substrate to facilitate imaging with traditional optical microscopy apparatus for cellular studies. The program has followed three parallel tracks: 1) lithography and processing of interconnect and seed metals and nanofabrication of the sites for locating the SWNTs, 2) SWNT fabrication and process integration with the interconnect levels, 3) development of SWNT functionalization strategies that are adaptable to the fabricated device.

Interconnect and seed metal processing was developed with the assumption that the SWNTs would be deposited using a CVD process.[2,3] A Cr/Co bilayer was deposited and patterned using photolithography on quartz wafers. A schematic of the process is shown in Fig. 1. The details of the process flow are reported in a Ph. D. dissertation.[4] The process starts with a quartz wafer (100 mm diameter by 350 μm thick). The process for the interconnect metal and SWNT seed growth follow from the work of Graham et al[5]

with some modifications. A thin of layer (20 nm) Cr is first deposited to improve adhesion to the substrate before depositing 120 nm of Co, which was to serve as seed metal for the SWNT growth in the original scheme. The metal stack also provides interconnects for the SWNT probes. The interconnect pattern was transferred to the metal using traditional contact photolithography and liftoff. The interconnect pattern is connected electrically to large pads at the periphery of the wafer. This facilitates grounding the metal during e-beam lithography. The electrical connections between different devices are made in the kerf (between each device) and are severed when the wafer is diced. The deposition of gold is optional and is intended to improve contact when the device is soldered to a circuit board. In practice it was determined that Co can be soldered directly to surface mount contacts on a PC board using indium solder. The layout on a wafer as shown in Fig. 2a yields 9 chips. Each chip has 5 sets of interconnect pairs that are separated by ~ 3 μm near the intended locations of the SWNTs as shown in Figs 2c and 2d.

The SWNT growth at the desired locations is achieved by depositing a thin layer (50 nm) of SiN_x on the metal stack and using either electron-beam lithography and reactive ion etching (RIE) or focused ion beam drilling to open up nanoscale windows (also called vias) to the metal where the SWNTs will be seeded. The thickness of the SiNx layer is limited because of the aspect ratio of the via and the etch resistance of the e-beam resist. After deposition and passivation of the SWNTs the deivce is surfaced mounted on a PC board with connections for each SWNT and two sets of test pads. A fully assemble device without SWNTs is shown in Fig. 2b. A glass tube (cut from a standard test tube) was mounted on the device so that liquid cell medium can be contained.

The design calls for one SWNT to be deposited on each of the interconnects on both sides of the ~ 3 μm gap so that a cell positioned over the gap will be contacted by two SWNTs. This concept was tested with live cells using a fully packaged device without SWNTs. Fig. 2e shows an HEK293 cell positioned over the gap using patch-

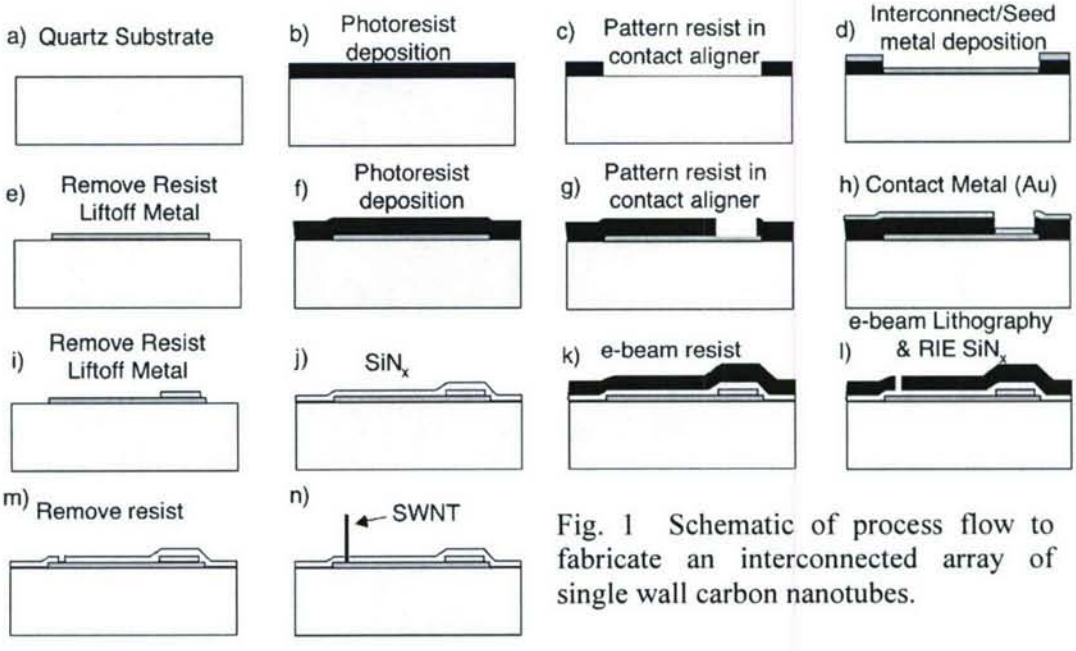

Fig. 1 Schematic of process flow to fabricate an interconnected array of single wall carbon nanotubes.

clamp cell micro-positioning apparatus. HEK293 cells were chosen since they are regularly used in studies of ion channels using patch-clamp techniques and will be the first cells measured in the completed device.

The integration of individual vertically aligned CNTs at precise locations is difficult because of the inevitable requirement of lithography at the scale of the diameter of the nanotube. Some success has been achieved using focused ion beam techniques for growing MWNTs using CVD. [6,7] Ideally, to obtain single vertically aligned SWNTs at precise locations using CVD, 1 to 2 nm vias should be opened in a layer covering the seed metal. Alternatively, single 1 to 2 nm seed metal particles should be deposited (or created lithographically) at precise locations. The practical minimum feature size in resist using e-beam lithography is approximately 20 nm. This is mostly limited by exposure of the resist to scattered electrons and the required thickness of resist to withstand the etch process for the SiN_x layer. An example is shown in Fig. 3 where a 150 nm thick layer of ZEP 520 resist was patterned. The minimum features size using focused ion beam techniques may be 5 nm and does not require a resist or etch process for pattern transfer. For this study only e-beam lithography results were available at the time of this report.

To get the smallest feature sizes possible in e-beam lithography it is necessary to find a process window that includes the RIE of the SiN_x. That is,

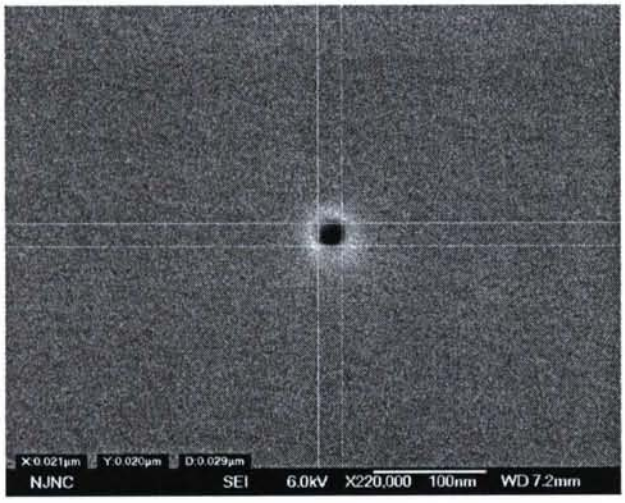

Fig. 3 SEM image of 20 nm via in 150 nm thick ZEP resist (e-beam sensitive) on 50 nm SiN_x/120 nm Co/20 nm Cr/quartz.

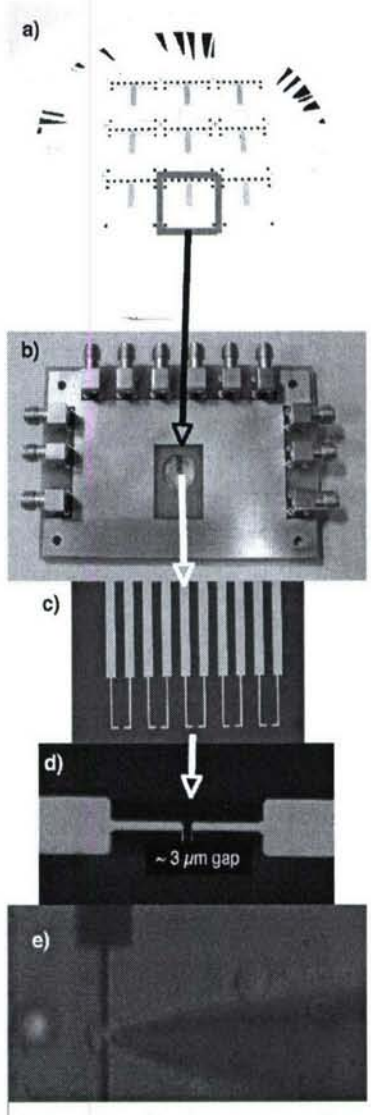

Fig. 2 a) Quartz wafer with interconnect/seed metal pattern, b) single chip surface mounted on underside of PC board for testing, c) 5 sets of 2 interconnects separated by ~ 3µm gap shown in d), and e) HEK293 cell positioned over contacts using a patch clamp micropipette.

several dose focus series must be performed. The difficulty with this optimization is determination of the performance of the resist and RIE independently, since imaging the resist in the SEM before RIE requires a conductive coating for these feature sizes with a sample that is largely insulating. A conductive coating (Au/Pd) was used to produce the SEM image in Fig. 3. These samples cannot be etched. Unfortuntely, without prior knowledge of the minimum feature size in resist it is difficult to fully characterize the RIE. When combined with the inevitable loss of resist during RIE, final feature sizes are generally larger after RIE than in resist. In the results reported here e-beam lithography was used to create vias with diameters from 5 nm to 100 nm in ZEP 520 resist (150 nm thick) and RIE using CHF_3 as a reactant was performed to open vias in the SiN_x. However, only 40 to 100 nm vias were observed and after etch the smallest vias were approximately 100 nm. That is, none of the vias were small enough to limit the number of grown or deposited SWNTs to only one or to limit the diameter of SWNTs. It is important to note that this is not the resolution limit of the e-beam lithography. These results only represent one dose focus result while developing the process. It is reasonable to assume that, after further refinement of the process, vias under 50 nm in diameter could be fabricated. However, the e-beam lithography results reported here were sufficient to demonstrate a powerful technique for depositing SWNTs.

Carbon Nanotube Deposition

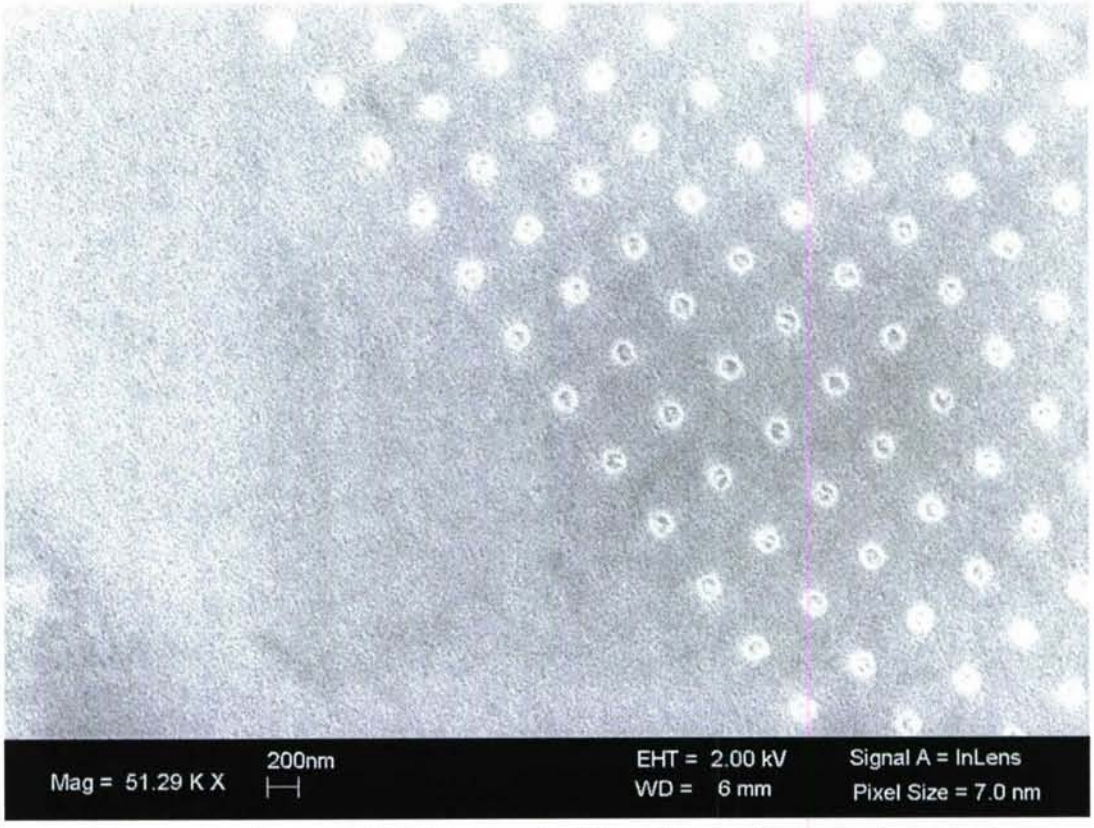

Fig. 4 SEM image of SWNTs deposited in ~ 100 nm diameter vias etched in 50 nm SiN_x/120 nm Co/20 nm Cr/quartz.

A significant effort was expended to derive a CVD process for growing vertically aligned SWNTs on the material stack used for this device. There were serious difficulties maintaining the thin SiN_x layer during CVD. It tended to not withstand the thermal cycles during CVD growth. A significant amount of cracking of the SiN_x was observed. This was in part because of the large thermal mismatch between the metal stack and the SiN_x. The CVD process was abandoned.

Presynthesized SWNTs were deposited within the vias. An example of the results are shown in Fig. 4. Fig. 4 is an SEM image of an array of ~ 100 nm diameter vias with deposited SWNTs. All of the vias were only partially filled and there were a significant number of vias that had only one SWNT (or small bundle) deposited in the via. The presence of SWNTs was verified using micro-Raman spectroscopy from selected areas that cover 3 X 3 arrays of vias. The Raman spectra match the results that were measured from the pristine SWNTs used for the deposition. A more detailed description of this deposition process has been submitted for publication.[8] Finite element modeling of the deposition process was used to show that it is possible to control both the number and placement of the SWNTs. This is a groundbreaking result that has broad implications for many technologies that may use nanotubes.

III. CONCLUSION

The original goals of this seedling research project were to fabricate and test a device that demonstrates the viability of measuring localized chemical and mechanical events within a living cell with molecular scale resolution. This is a project that has a very high risk because it requires pushing several technologies beyond their present limits. The most difficult of these is fabrication of the actual device because there is no reported combination of process technologies for producing carbon nanotubes with the required properties at predetermined locations on patterned interconnects. The original process scheme that was proposed, if successful, would have made incremental improvements in a few critical technologies and would have given a process for fabricating devices that would be suitable for research applications of cellular biophysics. The result of this program was to demonstrate this capability by deriving a method for depositing vertically aligned SWNTs at precise locations using lithography and process technology that is currently available in manufacturing. The properties of the deposited nanotubes can be controlled since they are presynthesized and therefore can be presorted by electrical properties. That is, metallic SWNTs can be separated from those that are semiconducting.[9,10,11,12] The bandgaps of semiconducting SWNTs can be further narrowed for device grade starting material that is specific to an application.[13] The combination of these capabilities represents a major breakthrough in nanofabrication. It paves the way for the original concept of an interconnected array of nanosensors for intracellular signaling measurements to move forward. However, there is still significant risk remaining in the device fabrication and the measurement of cell signaling events. This includes the critical process of passivating the deposited SWNTs, functionalization of SWNTs for specific measurement requirements, and the interaction of the SWNTs with the cell during the actual measurements. The possible advances to understanding cellular dynamics and the medical advances that may derive from it make this research well worth the risk.

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APPENDIX

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